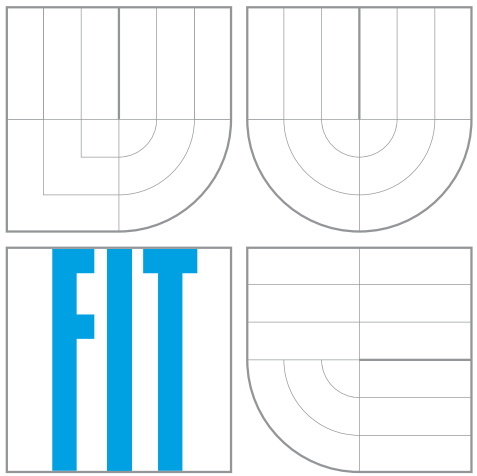
Non-Uniform CA Designer

FACULTY OF INFORMATION TECHNOLOGY

BRNO UNIVERSITY OF TECHNOLOGY



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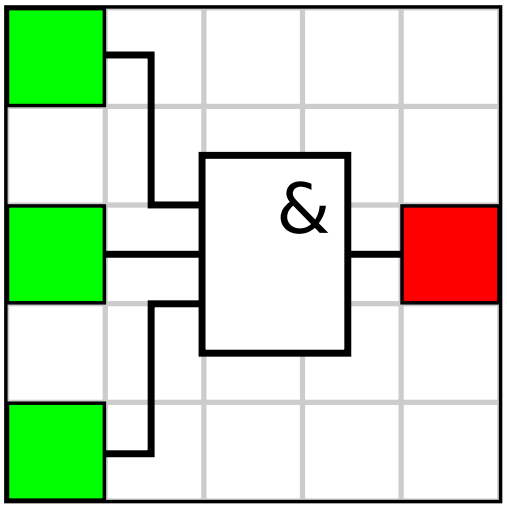
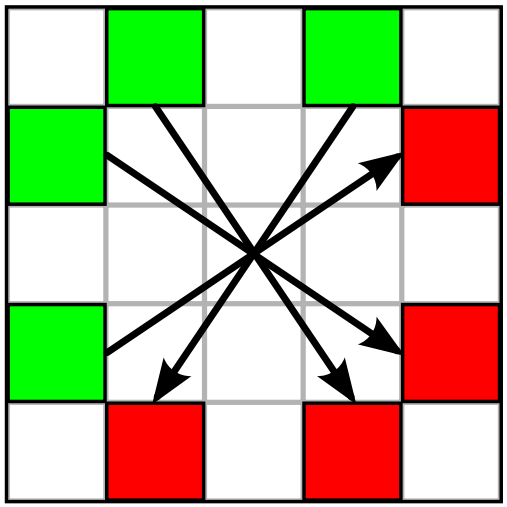
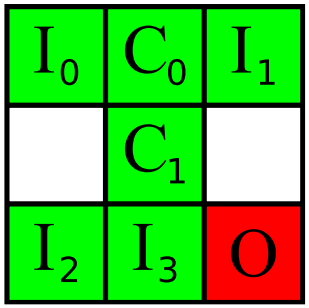
SUPERVISOR Ing. Michal Bidlo Ph.D.

Interpreting of Logical Gates by CA





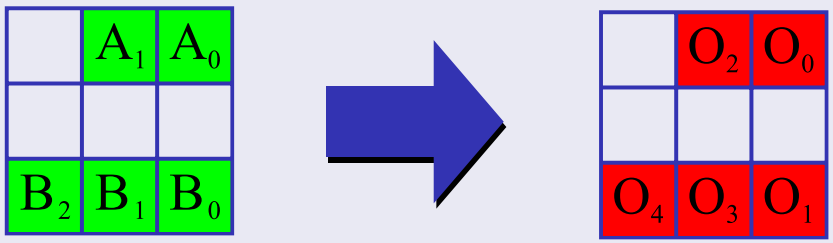
mux4



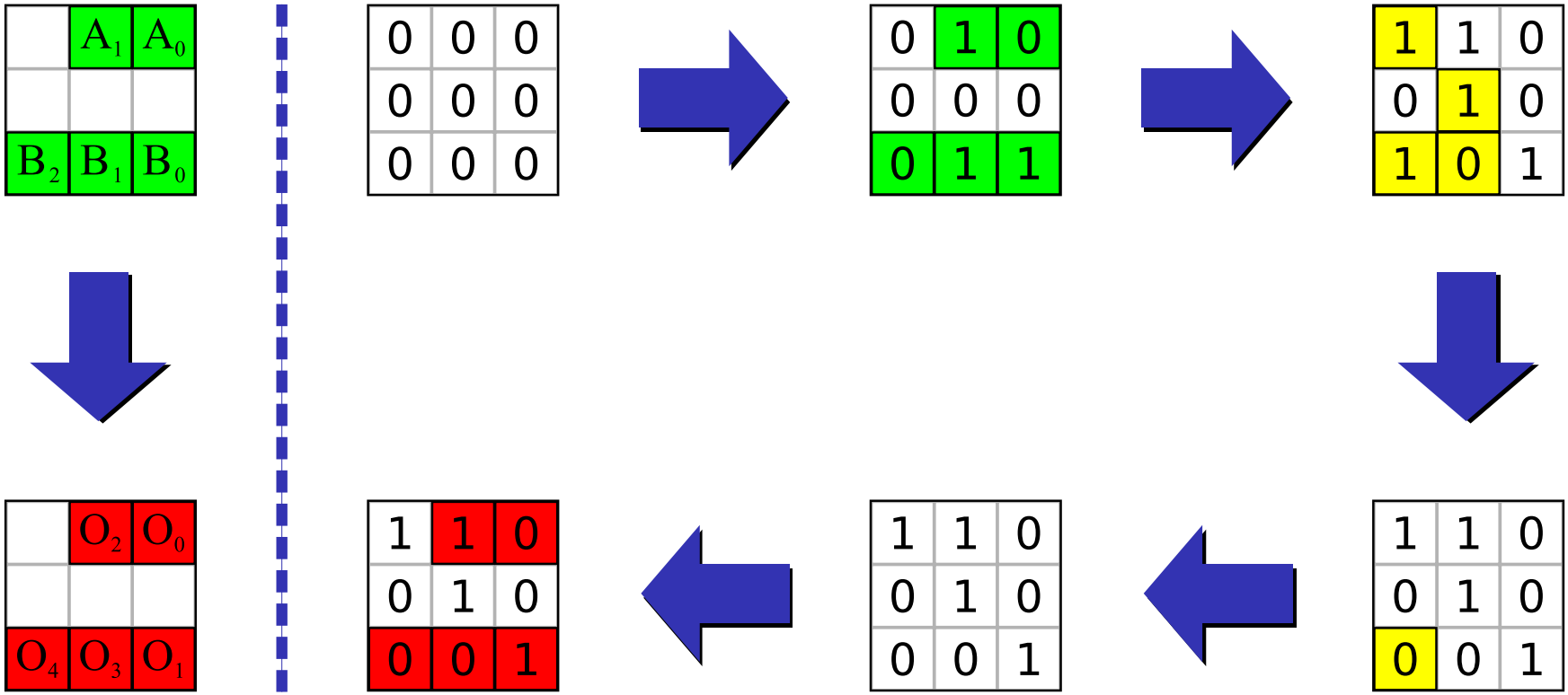
CA Simulator

- only **fully stable** solutions are accepted
- limit for count of steps (design parameter)
- the following CA stops in 1–5 steps for each input

Example: 2 × 3 bits **logical multiplier**



Example: 2 × 3 bits **logical multiplier** [input=0x0E]



CA Designer

- Hill Climbing
- automatic restart
- various genetic algorithms available (`GAlib`):
  - `GASimpleGA`
  - `GASteadyStateGA`
  - `GAIncrementalGA`
  - `GADemeGA`

  - http://lancet.mit.edu/galib-2.4/API.html

Found solutions

Circuit	**Variants**	**CA size**
AND, OR, XOR gates	2, 3 and 5 inputs	5×5
wire crossing	2, 3 and 2×2 wires	5×5
multiplexer	$4 + 2$ inputs	3×3
logical multiplier	2×3 bits	3×3

- **1024 solutions** per each of circuits above
- partial solutions of 3×3 bits logical multiplier

How to define a new circuit

- http://dudka.cz/nucad/html/api/index.html